

## MoNA/Sweeper Trigger bits

### Bit 0 (trigger pattern value = 1 if only bit set)

This bit is active if MoNA is enabled on the FPGA gui and singles, 1-fold, or two-fold is selected. This bit is never set if cosmics are selected. The bit will be set if the sum of the level 1 multiplicities (valid bars with cfd signals for both ends of a bar) is greater than or equal to the requested multiplicity and there is an external valid (either from a primary trigger or because self-enable is set on the gui). Note that singles is multiplicity=0 and this really means that there was at least one end of a bar that fired but there is no requirement that both ends have fired. This bit can be set with others but never with bit 2.

### Bit 2 (trigger pattern value = 4 if only bit set)

This bit is active if MoNA is enabled and cosmics are selected. This bit is never set if singles, 1-fold, or 2-fold is selected. The bit will be set if there are 3 or more valid bars in a single layer (as would be likely for most cosmic ray muons) and there is an external valid (primary trigger or self-enable). This bit can be set with others but never with bit 0.

### Bit 4 (trigger pattern value = 16 if only bit set)

This bit is active if a primary trigger is enabled and the primary singles box is selected on the FPGA gui. It will then be set for every primary trigger received. This bit is not exclusive. If a primary trigger is enabled, primary singles is selected, and MoNA 1-fold is selected then an event with a trigger and MoNA bar will result in bit 0 and bit 4 set (value of 17 for the bit pattern data word). If there is no MoNA present only bit 4 is set (value of 16).

### Bit 5 (trigger pattern value = 32 if only bit set)

This bit is active if a primary trigger is enabled and a downscale value is set. If the trigger is the nth trigger to be received, the event is valid and this bit is set. The bit is not exclusive. If MoNA is also enabled, a valid bar is found, and the primary trigger is the nth to be received at the FPGA (nth while the system is live; triggers while the system is busy are not counted) then bit 0 and bit 5 will be set for a value of 33.

### Bit 7 (trigger pattern value = 128 if only bit set)

This bit is set anytime there is an AUXC input and a trigger (or self trigger is enabled). It is not exclusive and may be found along with any of the bits listed above. Downscale primary trigger and AUXC will result in a value of 129. If there is a MoNA 1-fold, AUXC, and primary trigger downscale the trigger pattern will be 161.

### Bit 9 (trigger pattern value = 512 if only bit set)

This bit is set anytime there is an AUXD input and a trigger (or self trigger is enabled). It is not exclusive and behaves like bit 7.